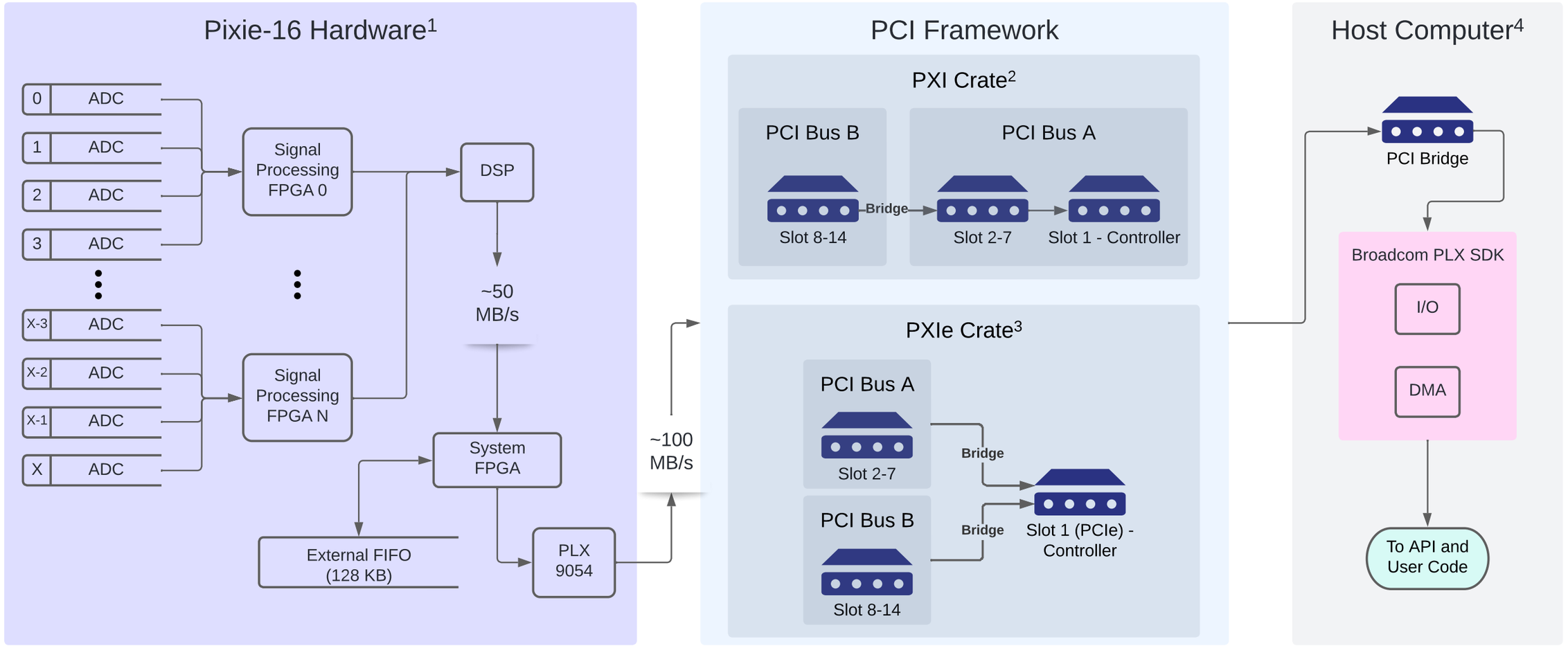


Legend

Data Synchronization Point

Asynchronous Data Store

Data Flow

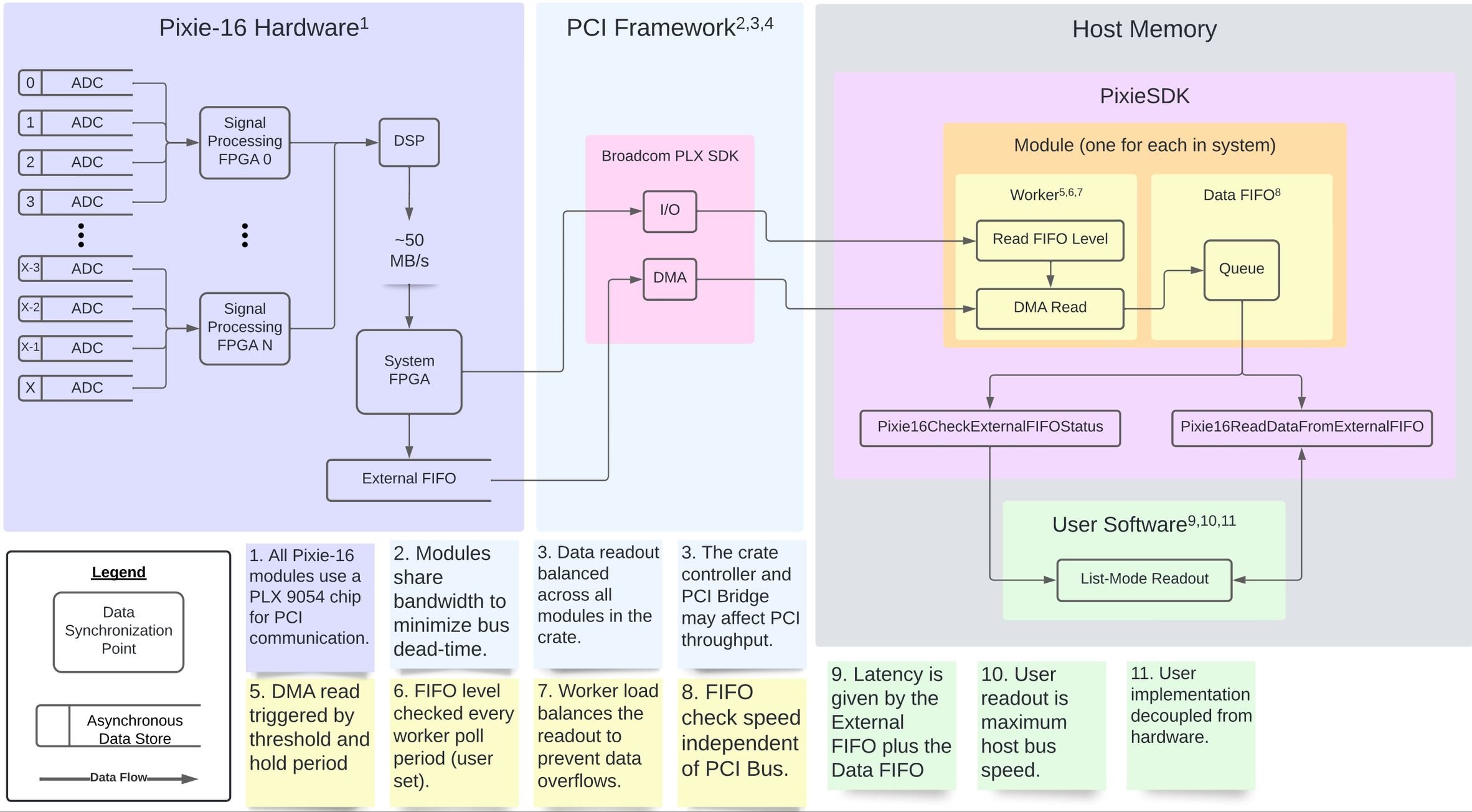
1. All Pixie-16 modules use a PLX 9054 chip for PCI communication.

2. All data from Bus B must flow through Bus A. This limits the throughput to ~100 MB/s.

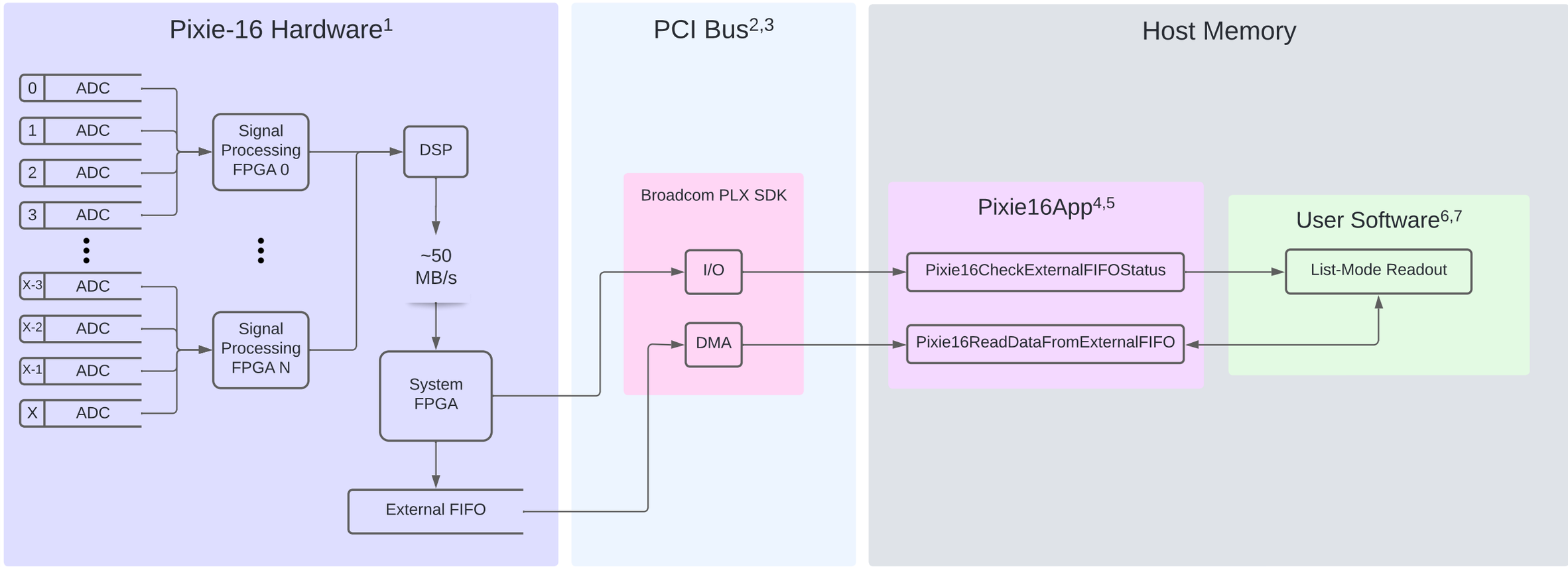
3. PXIe Crate's parallel buses allow ~200 MB/s transfer speeds.

4. The crate controller and PCI Bridge may affect PCI throughput.

XIA Instruments That Advance The Art	Pixie-16 List-Mode Data Flow Diagram - Hardware	Page: 1 / 4	Prepared By	Created On	Modified By	Modified On	Revision	For Public Release
			Stanley Paulauskas	2022-07-11	Stanley Paulauskas	2022-07-27	1.0.0	



XIA Instruments That Advance The Art	**Pixie-16 List-Mode Data Flow Diagram - PixieSDK**	Page: 2 / 4	Prepared By Stanley Paulauskas	Created On 2022-07-11	Modified By Stanley Paulauskas	Modified On 2022-07-27	Revision 1.0.0	**For Public Release**



Legend

Data Synchronization Point

Asychronous Data Store

Data Flow

1. All Pixie-16 modules use a PLX 9054 chip for PCI communication.

2. Serial readouts increase bus dead-time.

3. The crate controller and PCI Bridge may affect PCI throughput.

4. Calls are not thread safe.

5. Servicing one module at a time can lead to data loss.

6. Worst case latency and throughput driven by user implementation.

7. User implementation implicitly coupled to hardware changes.

XIA Instruments That Advance The Art	**Pixie-16 List-Mode Data Flow Diagram - Legacy API**	Page: 3 / 4	Prepared By Stanley Paulauskas	Created On 2022-07-11	Modified By Stanley Paulauskas	Modified On 2022-07-27	Revision 1.0.0	**For Public Release**