XMAP Pixel Advance Logic Configuration

During a mapping data acquisition run the pixel number and corresponding spectrum memory pointers advance under the control of an external timing signal. This short document is intended to assist you in connecting and configuring the pixel advance logic.

1. Pixel Advance Control

1.1. GATE Logic

The recommended method for advancing the pixel number is to use the GATE digital input both to synchronize the start of the run and to advance pixels. Optionally the GATE signal can halt data acquisition between pixels.

1.1.1. GATE-Veto vs. GATE-Ignore

Using an external signal to halt data acquisition is useful for two reasons: It is useful in multi-module systems, where a clean 'start run' procedure is desired: The GATE signal is held asserted while the software starts the run, then released such that all modules start simultaneously (see figures 1 and 2 below). Halting data acquisition between pixels enhances spatial discretization and reduces smearing effects. In the GATE-Veto mode, the GATE signal disables data at the beginning of the run *and* during subsequent assertions (see figure 1). In the GATE-Ignore mode, the GATE disables data taking *only* at the beginning of the run and runs continuously between pixels (see figure 2).

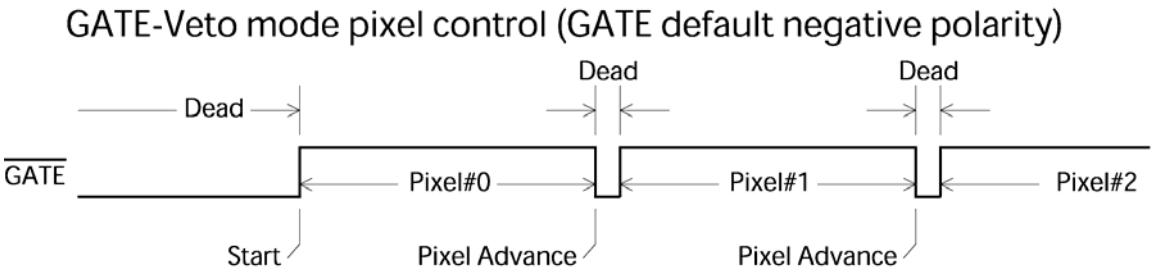

Figure 1: Gate-Veto mode halts data acquisition whenever GATE is asserted.

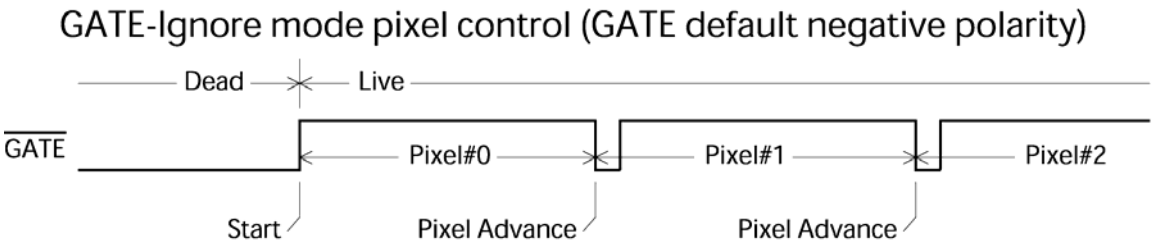

Figure 2: Gate-Ignore mode halts data only at the beginning of a run.

1.1.2. GATE Polarity

The polarity of the GATE signal can be set independently. Default negative polarity (as in the figures) means the GATE signal halts data when LO, and the pixel advance occurs on falling edges. Positive polarity means the GATE signal halts data when HI, and the pixel advance occurs on rising edges.

1.2. Host Control

It is also possible to advance the pixel via the PCI bus, i.e. via a Handel command. Manually advancing the pixels is not a practical method for real mapping applications because of host computer latency and because the command must be issued separately to each XMAP module, but it does provide an easy way to test mapping operations. The Handel Quick Start Guide describes this command in detail.

2. GATE Connections

2.1. PCI Bus Segments and Slots

Each PCI bus segment supports up to 8 slots. Larger PXI crates contain two or more internal PCI bus segments. Such crates have front-panel markings—vertical hash marks between slot identifiers—to indicate where the bus segment boundaries are, e.g. For the 18-slot crate shown in Figure 3, slots 1-6 are in bus segment 1; slots 7-12 are in bus segment 2; slots 13-18 are in bus segment 3.

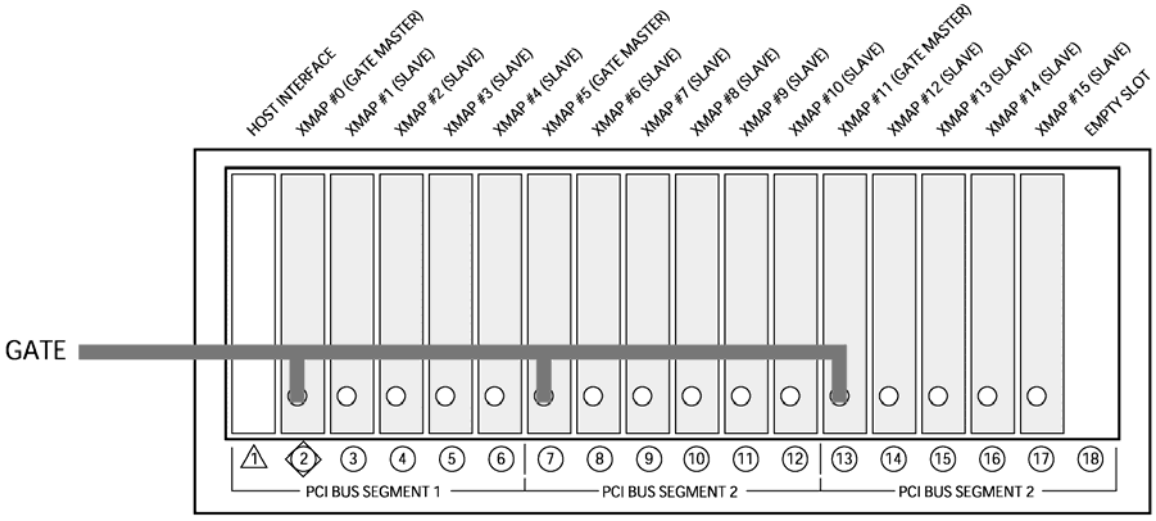

Figure 3: An 18-slot PXI crate containing host interface and 16 DXP-XMAP modules. The modules in slots 2, 7 and 13 are physically connected to the GATE LEMO cable. Modules 0, 5 and 11 thus should each be configured as a GATE Master. Modules 1-4, 6-10, and 14-17 should be configured as Slaves.

2.2. Master and Slave Modules

The front panel LEMO connector accepts the TTL/CMOS level GATE signal. It is not however necessary to connect a LEMO cable to each and every module in the system. Backplane PXI TRIG lines that span each bus segment can instead be used to propagate the GATE signal. If there are multiplie bus segments in your systems GATE must be physically connected to only one module—the Master—in each bus segment. The Master receives the LEMO input and drives the GATE signal onto a PXI TRIG line. Other modules in that bus segment—Slaves—receive GATE from the backplane PXI TRIG line. Each DXP-XMAP module must be configured via software as a Master or a Slave.